Exploring delay dynamics with a programmable electronic delay circuit

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(Received 10 October 2019; accepted 18 July 2020)

Delay dynamics occur in a wide variety of natural and man-made systems. Even simple delay systems can generate complex dynamics whose exploration is rewarding. To allow such exploration as part of advanced undergraduate laboratory courses and be able to utilize systems that operate at convenient timescales, it is necessary to delay analog signals by several milliseconds. In this paper, we describe an implementation of a programmable digital circuit capable of delaying DC-coupled analog signals up to 262 ms at a 1 MHz sampling rate. The initial history of the system may also be arbitrarily programmed, enabling the study of transient behavior. As an application, we discuss the use of this programmable delay in a feedback circuit that produces period-four triangular solutions, in complete agreement with theoretical predictions.

https://doi.org/10.1119/10.0001695

I. INTRODUCTION

Delay dynamics have wide relevance in fundamental science and technology. This is due to the ubiquitous presence of feedback loops in which delays arise because of natural processes[1] or control interfaces,[2,3] none of which are instantaneous. For example, many actuators, sensors, and communication networks contain feedback control loops that have non-negligible delays due to control loop processing times, buffering, and signal propagation delays. In addition, delays arise via model reduction techniques as simplified descriptions of complicated physical phenomena.[1,4]

In delay systems, the rate of change of a system will depend not only on its present state but also on its past states. This makes the dynamic behavior of delay systems rich and their exploration rewarding,[5] yet the implementation of convenient bench-top platforms to experimentally study delay dynamics can be challenging.

One challenge arises from the trade-off between experimentally convenient timescales of the dynamics and the ease of implementation of a programmable delay. One of the simplest ways to implement a delay is via signal propagation. However, delays achieved over reasonable propagation lengths are usually well below one microsecond because electronic signals in coaxial cables and optical signals in fibers propagate at roughly two-thirds the speed of light in a vacuum. This means that propagation delays are significant only if the internal dynamics of the delay system as a whole are fast, which, in turn, requires the use of sophisticated test and measurement equipment. An example of such fast bench-top systems is optoelectronic oscillators,[6–9] which may produce oscillations with frequencies in excess of 1 GHz. In contrast, for bench-top experiments that exhibit oscillations at convenient frequencies of a few kilohertz, the required delays are on the order of several milliseconds. Controllable millisecond-delays of analog signals are difficult to achieve via propagation but can be obtained by dedicated delay circuits.

In this paper, we detail the implementation of one such delay circuit. Our controllable delay circuit (see Fig. 1) is based on first in, first out (FIFO) memory, and achieves precise and large delays up to several hundred milliseconds. While commercial audio equipment with programmable millisecond delay is available, these devices are mostly AC-coupled.[23] One of the advantages of our circuit is that it is DC-coupled, allowing constant voltages to pass through. Our circuit is also able to program the initial memory of the FIFO, giving the experimenter full control over the initial state of the system.

The paper is organized as follows: in Sec. II, the implementation of the programmable delay is explained and its performance is characterized; in Sec. III, an application is described in which the delay circuit is used to create a simple delay dynamical system; and in Sec. IV, possible extensions of this work are discussed.

II. A PROGRAMMABLE DELAY FOR ANALOG SIGNALS

Our circuit delays signals by a user-set number of periods of an external clock input. Each clock cycle, the circuit's analog to digital converter (ADC) samples the input signal

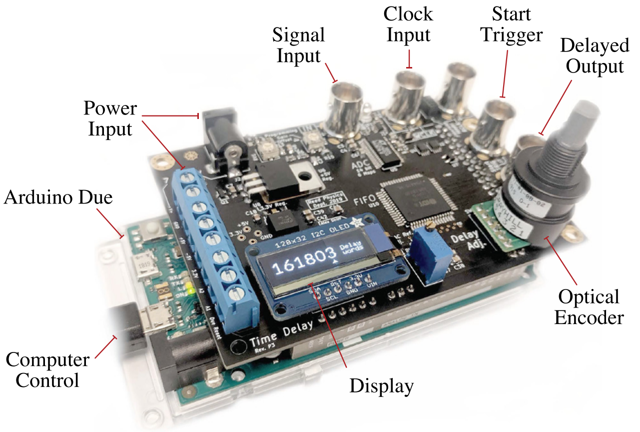

Fig. 1. The assembled time delay circuit, mounted on top of an Arduino Due.

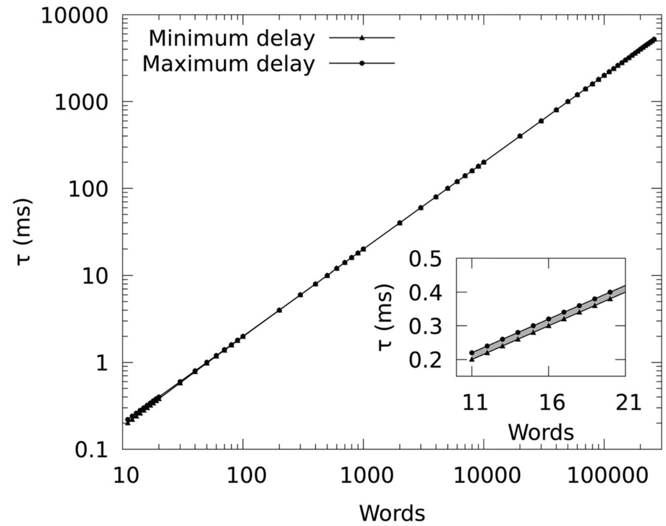

Fig. 3. Measured extrema of delay as a function of the number of words specified. A 10 Hz square signal and a clock of 50 kHz were used. The time delay is precisely linear in the number of words. The shaded region (visible in the zoom shown as the inset, essentially invisible in the main figure) is the measured uncertainty in the delay, which is no more than that introduced by sampling the input signal (see the text).

and stores the resulting 14-bit word in FIFO memory. After the specified number of clock cycles, the word is read from the FIFO and converted back to an analog signal by a digital to analog converter (DAC). This path is depicted in Fig. 2.

The number of words of the delay (i.e., number of clock cycles) can take any value within the allowed range of 11–2^{18} words and is set by the user either via an optical encoder on the circuit or via a computer that is connected through a USB cable to the Arduino Due (see Fig. 1). The value of the chosen delay is displayed on a screen. The user also provides the external clock signal, which sets both the sampling rate of the analog input signal and the actual delay, the latter being the product of the clock period and the chosen number of words. The circuit has been verified to produce the expected delays for clock frequencies up to 6 MHz.

The delay is perfectly linear over the full delay range of possible delays, as demonstrated in Fig. 3.[24] The uncertainty in the delay is found to be one clock period or less, as seen in the inset of Fig. 3 by the shaded region between the maximum and minimum measured delay with a vertical extend of 20 μs, corresponding to the clock period of $(50\,\text{kHz})^{-1}$. This uncertainty unavoidably occurs because one clock period is the resolution limit with which the circuit can determine the time of level transitions of a square wave input signal, such as the one used for the delay measurement in Fig. 3.

The circuit also supports programming of the initial memory of the FIFO, giving the experimenter full control over the initial history of the system being studied (Fig. 4). An analog switch and additional control logic allow the analog output from an Arduino Due to be connected to the input of the ADC. The Arduino Due is sent the initial memory words from a computer. The Arduino Due then alternately outputs and clocks in the words to the ADC and FIFO, filling the memory. Finally, the Arduino Due returns the analog switch back to the default position, connecting the external input to the ADC, sets the delay, and lets the external clock input control the timing of the delay circuit, as explained above.

The output from the DAC inherently has glitches when many bits of the output change, such as when the signal crosses zero. These glitches and some noise are removed by

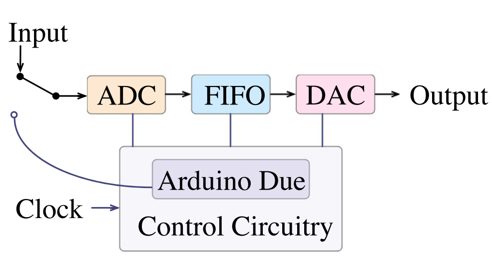

Fig. 2. Block diagram of the circuit. The input signal is digitized by a 14-bit ADC, delayed by the FIFO, and then converted back to an analog signal by a 14-bit DAC. The Arduino Due and other control circuitry configure the number of delay words and enable the initial memory of the FIFO to be programmed through the ADC.

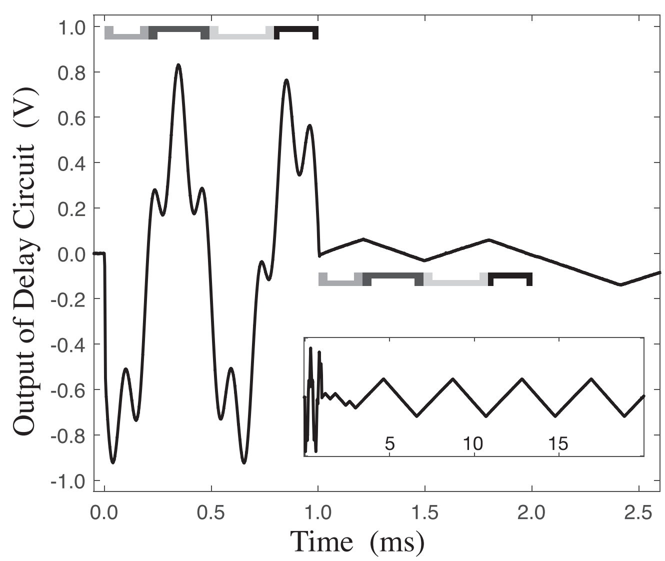

Fig. 4. The delay circuit was programmed with 6000 words of history and then switched into the self-feedback circuit that is depicted in Fig. 7 and discussed in Sec. III. The clock rate was 6 MHz, such that the 6000 word delay corresponds to a physical delay of 1 ms. The transient signal shown was measured at the output of the delay circuit (V_τ in Fig. 7), such that the first millisecond of the signal is the programmed history, whereas the subsequent triangular-type signal is due to the feedback-circuit delay-dynamics resulting from this history. Inset: beyond approximately 3.6 ms, the output becomes a regular triangle wave with a period of 4 ms.

adding a low-pass filter to the output. Whereas a simple 100 kHz single-pole low-pass filter was able to remove the glitches, we used an active 121 kHz fourth-order Bessel low-pass filter for its improved attenuation and maximally flat group delay. This provides good filtering with minimal distortion of the signal, as demonstrated in Fig. 5.

In summary, our programmable delay circuit is convenient, flexible, and produces high-quality delayed analog signals. Additional details about the circuit operation can be found in the supplementary material.[26]

III. APPLICATION: EXPLORING THE DYNAMICS OF DELAY DIFFERENTIAL EQUATIONS

As a possible use of the programmable delay in advanced undergraduate laboratory classes, we discuss a circuit that incorporates the delay and generates triangle waves. Not only is the circuit straightforward (aside from the delay circuit), but the circuit dynamics are described by a simple delay differential equation for which, rather remarkably, solutions can be found analytically. The study of this circuit and its dynamics provides, therefore, an excellent point of departure for exploring the rich landscape of delay systems.

A. Theory

Delay differential equations (DDEs) are differential equations where the derivative depends on the solution at prior times. Autonomous scalar DDEs with a single constant delay are a simple example and have the form

$$\frac{\mathrm{d}x}{\mathrm{d}t'} = f\big(x(t'),\, x(t'-\tau')\big), \tag{1}$$

where the time delay τ' is a positive constant and f is a function of both x at this time and x a time τ' in the past. In contrast to ordinary differential equations, for which it is sufficient to specify initial values at a single initial time, DDEs require an initial history function. That is, to obtain a

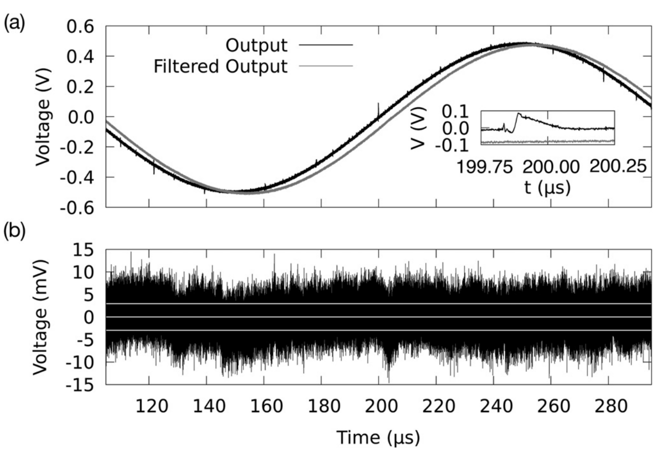

Fig. 5. (a) A 5 kHz, 1 Vpp sine wave is delayed by 1000 periods of a 5 MHz clock. The glitches in the output (black, zoom in the inset) are removed by a fourth-order Bessel filter (result in gray), which adds an additional delay of its own. (b) Residual, i.e., input–output difference after filtering and shifting by the total delay. This difference (depicted) has a mean of $-7.5\,\mu$V and a standard deviation of 3.0 mV, which are indicated by horizontal lines. The essentially flat residual (up to random noise) demonstrates that our circuit does not significantly distort signals.

unique solution of Eq. (1) for times $t' > 0$, one needs to specify the functional form of $x(t')$ on the entire interval $[-\tau', 0]$.

As one of the simplest nonlinear DDEs, consider the following scalar DDE with negative feedback

$$\frac{\mathrm{d}y}{\mathrm{d}t} = -f(y(t-1)), \tag{2}$$

where f is defined as

$$f(y) := \begin{cases} -1 & \text{if } y < 0 \\ 1 & \text{if } y \geq 0. \end{cases} \tag{3}$$

In order to keep the theory general, Eqs. (2) and (3) are written in terms of dimensionless quantities. The signal is represented by the dimensionless variable y, which is scaled such that the step nonlinearity f has an output of ± 1. Dimensionless time has been introduced as $t = t'/\tau'$, resulting in a dimensionless delay of $\tau = 1$.

Step nonlinearities, such as Eq. (3), arise in certain control problems with so-called relay controllers. Relay control provides a simple "on" or "off" feedback, which allows the use of simple and inexpensive actuators and imposes minimal requirements on the measurement of the system because only the sign of the signal needs to be observable. Although versions of the above system are therefore of practical interest, our motivation for considering Eq. (2) is that this DDE is easy to implement as a circuit and can be solved explicitly,[10,11] thereby providing a good introduction to DDEs and a convenient test case for the programmable delay.

In the following, we will show that solutions of Eq. (2) can be found by piecewise integration: we assume that a continuous initial function is specified on the interval $[-1, 0]$. One observes that solutions of Eq. (2) for $t > 0$ are piecewise linear in t, because the right-hand side of Eq. (2) is equal ± 1 with the timing of sign switches determined by zero crossings of the solution a delay time $\tau = 1$ in the past. It turns out that the solutions of interest have a period that is larger than the delay. They are called slowly oscillating, which is defined as follows: a continuous function $y : \mathbb{R} \to \mathbb{R}$ is called slowly oscillating at t if either $|y| > 0$ on $[t-\tau,\ t]$, or y has precisely one zero at $t^* \in [t-\tau,\ t]$, $\dot{y}(t^*)$ exists and $\dot{y}(t^*) \neq 0$.

Consider Fig. 6(a), where a slowly oscillating initial function is shown that is zero at $t = 0$ and negative on $[-1, 0)$. Then, as depicted, piecewise integration of Eq. (2) results in the slowly oscillating period-four solution

$$g_0(t) = \begin{cases} \hat{t}, & 0 \leq \hat{t} < 1 \\ 2 - \hat{t}, & 1 \leq \hat{t} < 3\,, \\ \hat{t} - 4, & 3 \leq \hat{t} < 4 \end{cases} \quad \text{where } \hat{t} \equiv t \bmod 4. \tag{4}$$

Next, we argue that any bounded slowly oscillating function will remain slowly oscillating and will converge in finite time to $g_0(t + \varphi)$, where φ is a phase shift. To show this, we consider in turn three possible cases of slowly oscillating initial functions:

(I) If the initial function is zero at $t = 0$ and negative on $[-1,\ 0)$, then piecewise integration results in $g_0(t)$ for $t > 0$, as already shown. If the initial function is zero at $t = 0$ and positive on $[-1,\ 0)$ (Fig. 6(b)), then

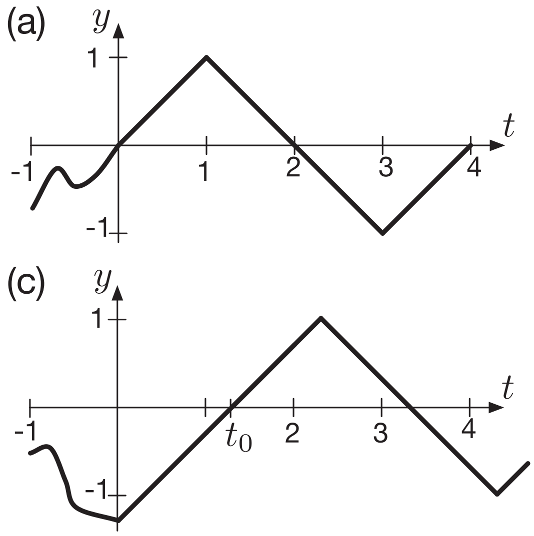

Fig. 6. Slowly oscillating solution ($\tau = 1$): (a) case I with a negative initial function, (b) case I with a positive initial function, (c) case II, and (d) case III.

piecewise integration results in $g_0(t+2)$. The same solution but shifted by $\varphi = 2$.

(II) If the initial function is nonzero on the entire interval $[-1, 0]$ (Fig. 6(c)), then, under forward integration, the magnitude of y for $t > 0$ will decrease from the value $|y(0)|$ at $t = 0$, such that the solution will first be zero at the instance $t_0 = |y(0)|$, reducing this case to case I. The solution is $y = g_0(t + \varphi)$ for $t > t_0$ with either $\varphi = -t_0$ if y is negative on $[-1, 0]$ or $\varphi = 2 - t_0$ if y is positive on $[-1, 0]$.

(III) Finally, if the initial function has one zero crossing t^* on the interval $[-1, 0)$ but is nonzero at $t = 0$ (Fig. 6(d)), then the solution has the next zero crossing at the instance of time $t_0 = 2 - 2|t^*| + |y(0)|$ and no zero crossing on $[t_0 - 1, t_0)$. As in case II, the solution is $y = g_0(t + \varphi)$ for $t > t_0$ with either $\varphi = -t_0$ if y is negative on $[-1, 0]$ or $\varphi = 2 - t_0$ if y is positive on $[-1, 0]$.

This shows that a slowly oscillating initial function can never yield a solution with more than one zero crossing on a unit time interval, the solutions remain slowly oscillating. More importantly, any slowly oscillating initial function converges to the period-four solution (4) in finite time. Moreover, it can be shown that any bounded continuous initial function, slowly oscillating or not, will converge in finite time to the period-four solution; the only exception is a set of unstable so-called fast oscillating periodic solutions. This can be demonstrated using familiar tools from linear algebra (as shown in the supplementary material[26]). Therefore, any experiment described by Eq. (2) should yield the period-four triangle solution g_0 in Eq. (4) after initial transients have died out.

B. Experiment

The DDE circuit shown in Fig. 7 consists of three functional blocks: the delay, nonlinearity, and integrator. The dashed block implements the step-nonlinearity f given by Eq. (3). Within this block, the first operational amplifier's output is the negative (positive) rail voltage for positive (negative) inputs. The second operational amplifier centers the rail voltages with respect to ground and scales the output amplitude to $V_0 = 500$ mV. The resulting signal is integrated by the third operational amplifier. Finally, the integrator output is fed back and delayed by τ' via the programmable delay. The integrator output is given by

$$V_{\text{out}}(t') = -\frac{V_0}{RC}\int_0^{t'} f(V_{\text{out}}(s - \tau'))\mathrm{d}s. \tag{5}$$

It should be noted that Eq. (5) maps onto Eq. (2) if one differentiates Eq. (5) and introduces the dimensionless time $t = t'/\tau'$ as well as the dimensionless variable

$$y = \frac{V_{\text{out}}}{V_0}\frac{RC}{\tau'}. \tag{6}$$

One therefore expects the circuit to produce the triangular solutions predicted by Eq. (4) in Sec. III A.

Figure 8 shows the measured output voltage V_{out} for three delay values with the three time series aligned such that $V_{\text{out}} = 0$ V at $t' = 0$ s. It is seen that the experiment indeed produces triangular period-four slowly oscillating solutions in full agreement with theoretical predictions. Furthermore, the amplitude of V_{out} scales with the delay in accordance with Eq. (6).

Further agreement with theory is found by looking at the startup behavior of the circuit. An example is shown in Fig. 4, which depicts the output V_τ (see Fig. 7) for a delay of 1 ms. The initial history that was programmed into the delay circuit corresponds to the first millisecond of output. After that, the data corresponds to the dynamics generated by the autonomously running circuit. In perfect agreement with theory, the circuit produces a constant positive slope when the

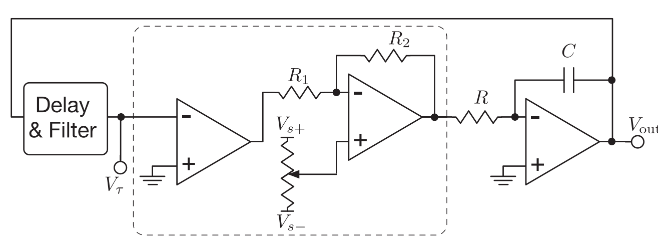

Fig. 7. Schematic of the DDE circuit. $R = 9.98$ kΩ *and* $C = 10.1$ nF.

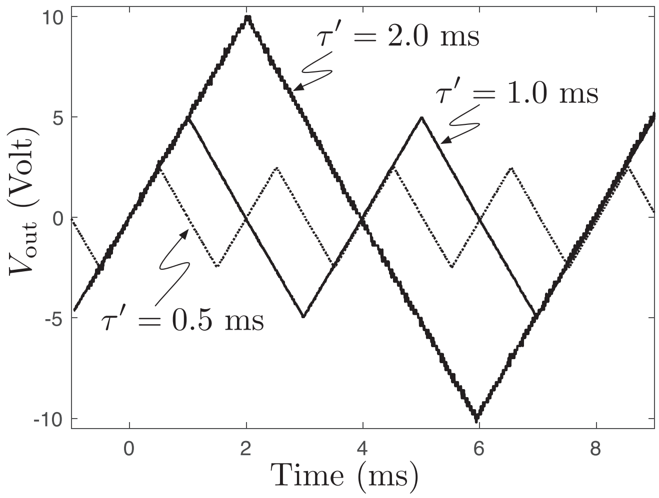

Fig. 8. Output generated by the DDE circuit for three values of the delay.

signal one millisecond prior is negative and produces a constant negative slope when the signal one millisecond prior is positive. As a guide to the eye, intervals in the initial data that are negative are indicated in Fig. 4 by light gray ⊔ shapes, whereas positive initial voltages correspond to dark gray ⊓ shapes. The resulting pattern ⊔⊓ is repeated underneath the output one millisecond later, confirming correct temporal alignment of the positive and negative slopes. As shown in the inset of Fig. 4, in just a few milliseconds, the circuit converges exactly to the expected 4 ms triangular period-four slowly oscillating solution.

IV. CONCLUSION

The delay circuit described in this work is a simple to use, flexible, and highly accurate implementation of a programmable analog signal delay. It is DC-coupled and allows the programming of the initial waveform residing in the delay memory; both of these features are lacking in most commercially available delays. The circuit is designed to strike a balance between accuracy and ease of use on the one hand and technical sophistication of implementation on the other hand. Designed to operate at clock rates below 6 MHz, a standard four-layer printed circuit board and proper layout is sufficient to guarantee signal integrity on a single analog-digital mixed signal board that includes the ADC, FIFO, and DAC chips. This makes the circuit relatively compact and inexpensive but limits the frequency of analog signals that can be delayed to below 100 kHz.

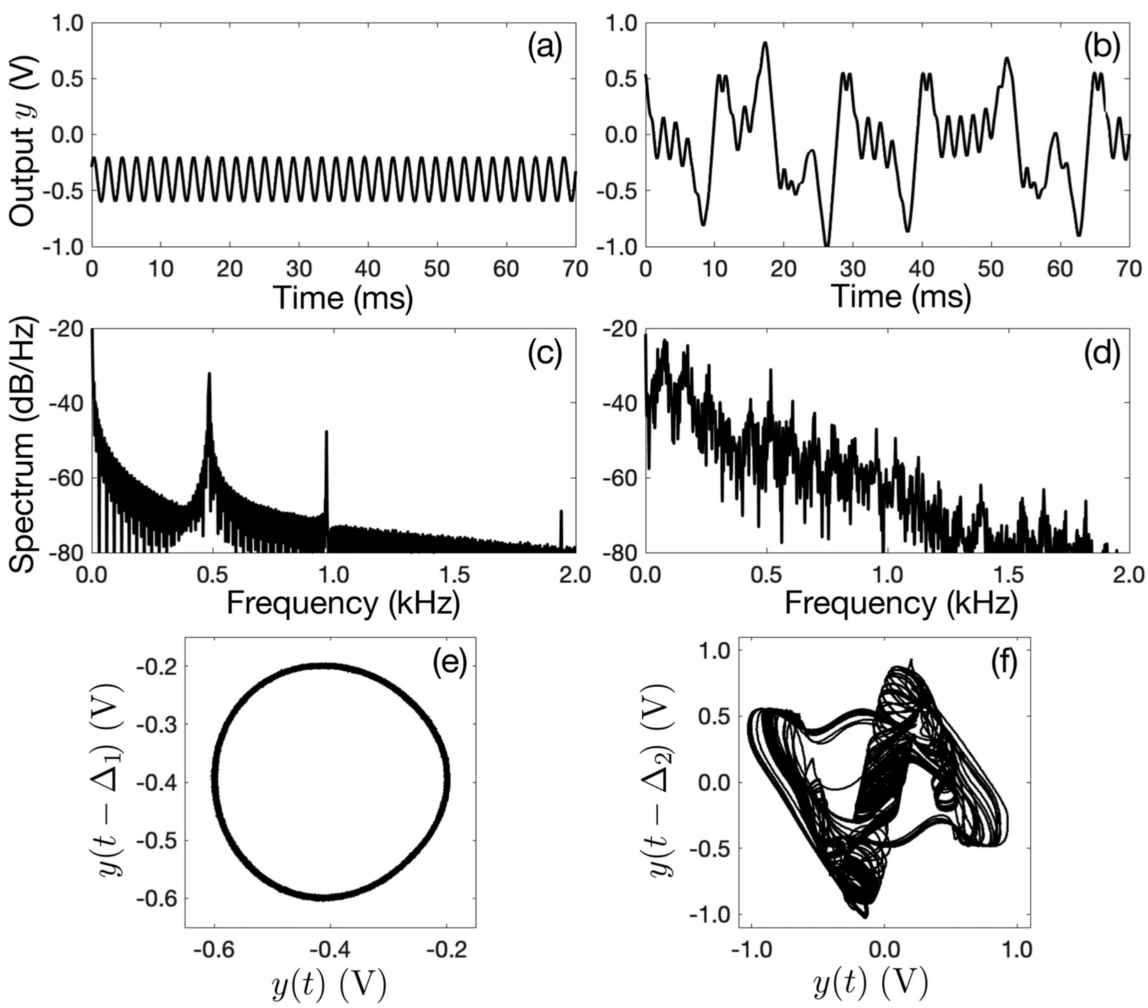

Fig. 9. Output generated by a DDE circuit with Rulkov–circuit nonlinearity: periodic dynamics [(a), (c), and (e)] and non-periodic, potentially chaotic, dynamics [(b), (d), and (f)]. Segment of the measured time series [(a) and (b)], estimate of the power spectral density [(c) and (d)], and delay embedding with $\Delta_1 = 0.51$ ms and $\Delta_2 = 2$ ms [(e) and (f)].

There are many potential uses of the delay circuit. In this paper, we have shown one example, the exploration of a simple nonlinear delayed feedback circuit. The feedback circuit's behavior is modeled accurately by a simple scalar delay differential equation, Eq. (2), which has the remarkable feature that it can be solved exactly. Our simple example is meant to demonstrate that delay systems are ripe for numerical, analytical, and experimental exploration that offer exceptional research projects for junior- or senior-level students.

Going beyond the simple example in Sec. III, more interesting and complex dynamics can be generated with the feedback circuit quite simply by changing the type of nonlinearity or by bandpass filtering the feedback signal.[5,8] The resulting delay dynamical systems tend to have rich bifurcations, nontrivial basins of attraction,[8] and can generate signals ranging from periodic and quasi-periodic oscillations[12] to chaos.[13]

An illustration of such rich behavior is shown in Fig. 9. The depicted dynamics were generated by the DDE circuit in Fig. 7 but with the step-nonlinearity replaced by a Rulkov-circuit nonlinearity.[14] Short segments of two measured time series are seen: a periodic waveform in Fig. 9(a) and a non-periodic waveform in Fig. 9(b). The periodicity of the first waveform is confirmed by the power spectral density estimate, shown in Fig. 9(c), which has a dominant peak at 0.49 kHz that rises well above the noise floor. Periodic dynamics is furthermore confirmed by the limit-cycle attractor that is seen when delay-embedding the time series by plotting the signal $y(t)$ versus a delayed version $y(t-\Delta_1)$.[15] In contrast, the second waveform has the experimental hallmarks of chaos. Namely, the spectrum has power at all frequencies well above the noise floor [as seen by comparing Figs. 9(d) and 9(c)] and a plot of the signal versus a delayed version shows a complicated (potentially fractal) attractor. The two time series are from the same circuit, the only difference being an increase in the delay time from 0.5 ms to 1.3 ms. The great variety of other dynamics that is generated by this circuit remains to be explored.[25]

Not only can delayed feedback destabilize systems,[16,17] leading to complex dynamics, but it can also have the opposite effect and be used as control,[18] stabilizing desired solutions.[3,19,20] Going even further, several such feedback systems could be coupled to form a network, enabling students to explore chaos synchronization[21,22] and other nontrivial emergent behaviors of networks. Clearly, the range of possible projects is vast and many of these projects will quickly reach the edge of what is currently known, allowing students to contribute original research.

ACKNOWLEDGMENTS

E.P. was supported in part by the Reed College Science Research Fellowship.

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[23]AC stands for alternating current and DC for direct current. A device input is called AC-coupled if the device only accepts oscillatory signals and suppresses or filters out constant inputs. It is called DC-coupled if the device accepts both constant and oscillatory signals. Audio equipment usually only processes AC-signals audible to humans, roughly 20 Hz to 20 kHz; it is AC-coupled.

[24]For the 1 Vpp square wave signal used for the delay measurement, the delay circuit output had a measured risetime of 129.1(3) ns. The relatively slow 50 kHz clock frequency was chosen to minimize contributions to the delay due to this finite rise time. This limited rise time due to the DAC is not an issue for continuous kHz-frequency signals.

[25]To the best of our knowledge, the dynamics of a Rulkov–circuit nonlinearity with time-delayed feedback has not been studied.

[26]See the supplementary material at https://doi.org/10.1119/10.0001695 for additional details about the circuit operation.